



8-Point Discrete Fourier Transform by Paired Representation

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Overview

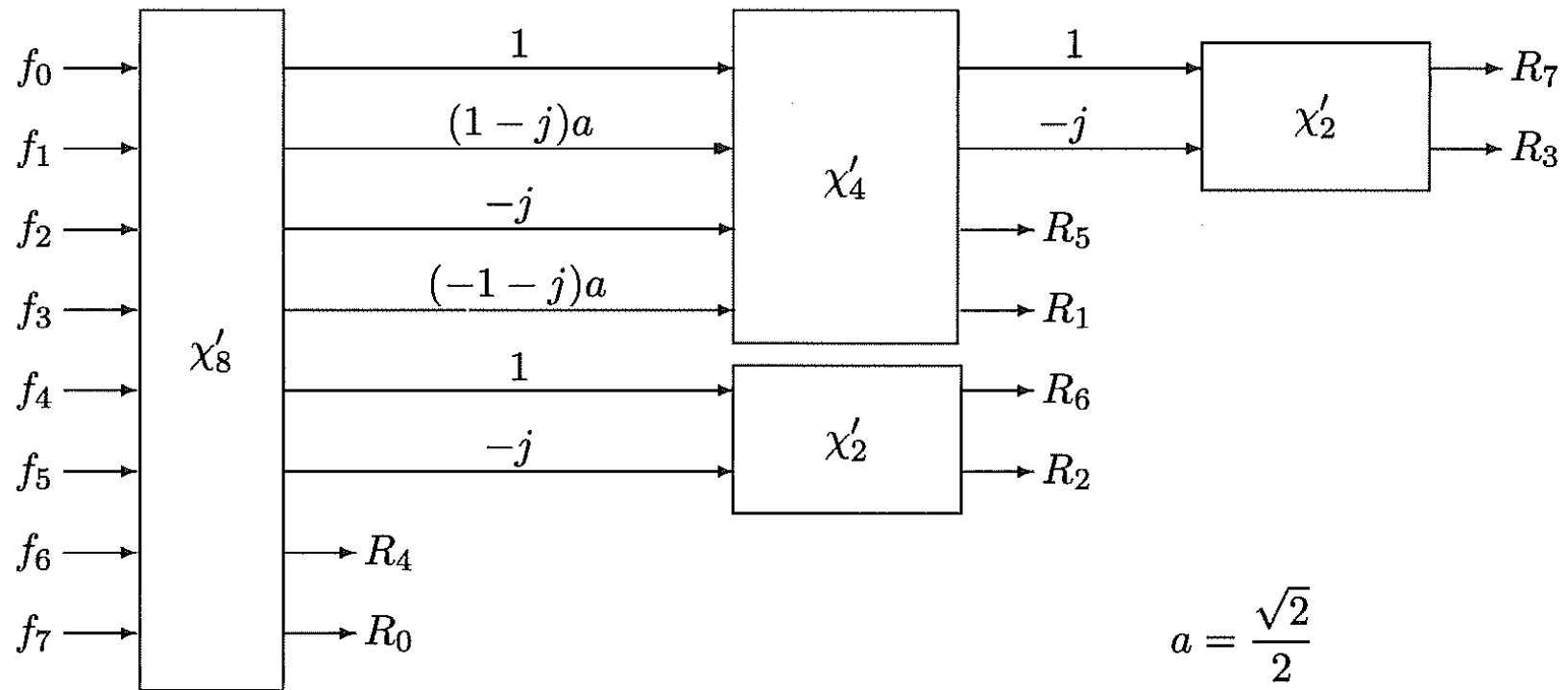
- Background
- DSP Algorithm
- Implementation
- Simulation Results
- Accuracy Check
- Realization
- Improvement
- Conclusion



Background

- DFT transforms discrete time signal to discrete frequency signal
- DFT requires $N*N$ complex multiplications
- Paired Representation used to reduce the number of calculations

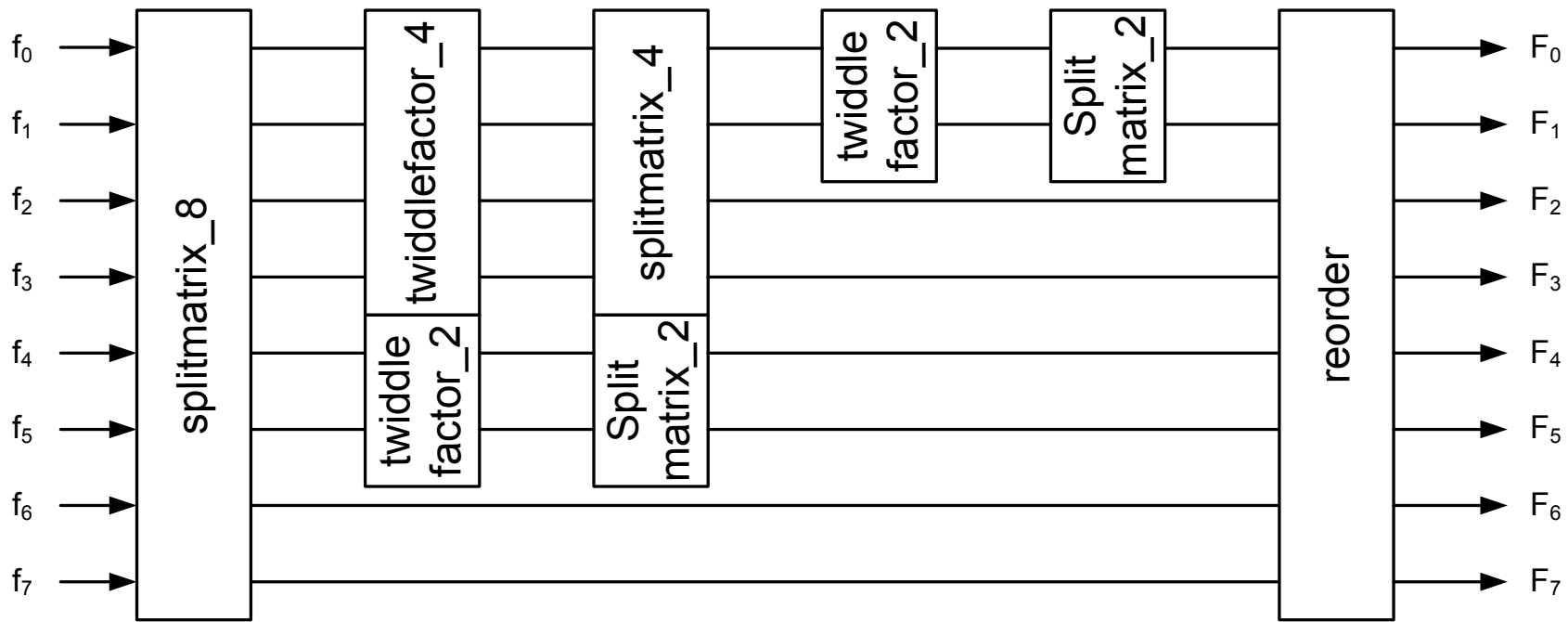
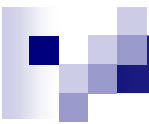
8 Point DFT by Paired Representation



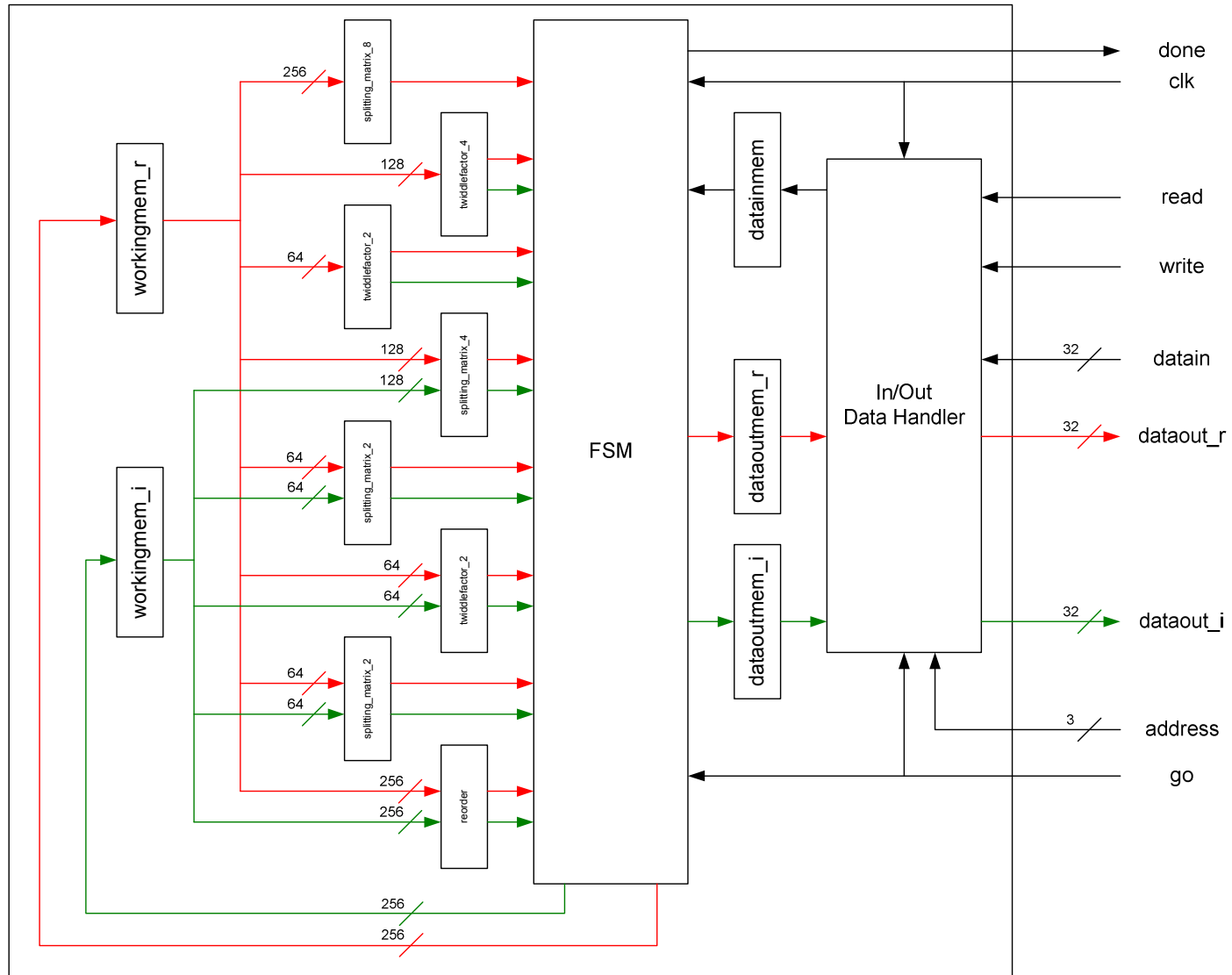


Implementation

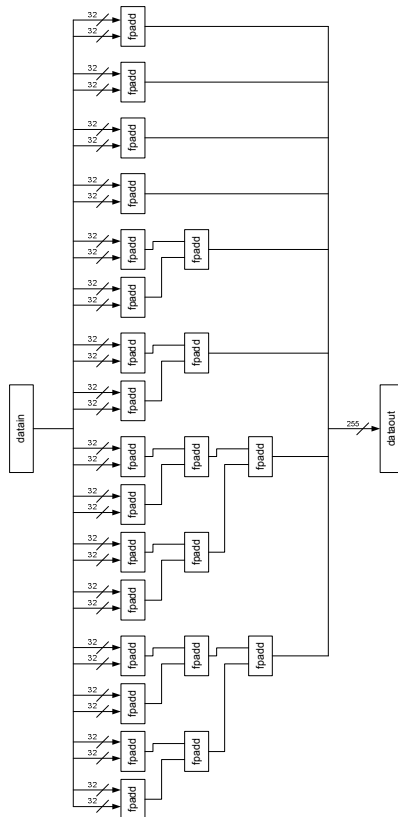
- All data represented in single precision floating point format (IEEE-754).
- All data is clocked in and out.
- 3 bit Finite State Machine



Block Diagram



Splitting Matrix



$$\begin{bmatrix} 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \\ 1 & 0 & -1 & 0 & 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 & 0 & 1 & 0 & -1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

- Matrix Multiplication
- Trivial multiplications result in only addition and subtraction operations.
- Must be repeated for both real and complex components

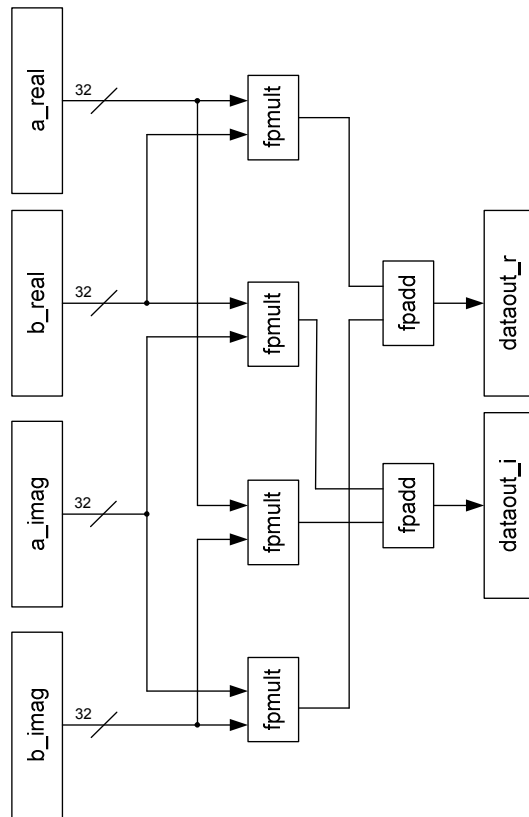


Twiddle Factor

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & \frac{\sqrt{2}}{2} - \frac{\sqrt{2}}{2}j & 0 & 0 \\ 0 & 0 & -j & 0 \\ 0 & 0 & 0 & -\frac{\sqrt{2}}{2} - \frac{\sqrt{2}}{2}j \end{bmatrix}$$

- Matrix multiplication with non-trivial terms.
- Requires to use a complex multiplier.

Complex Multiplier

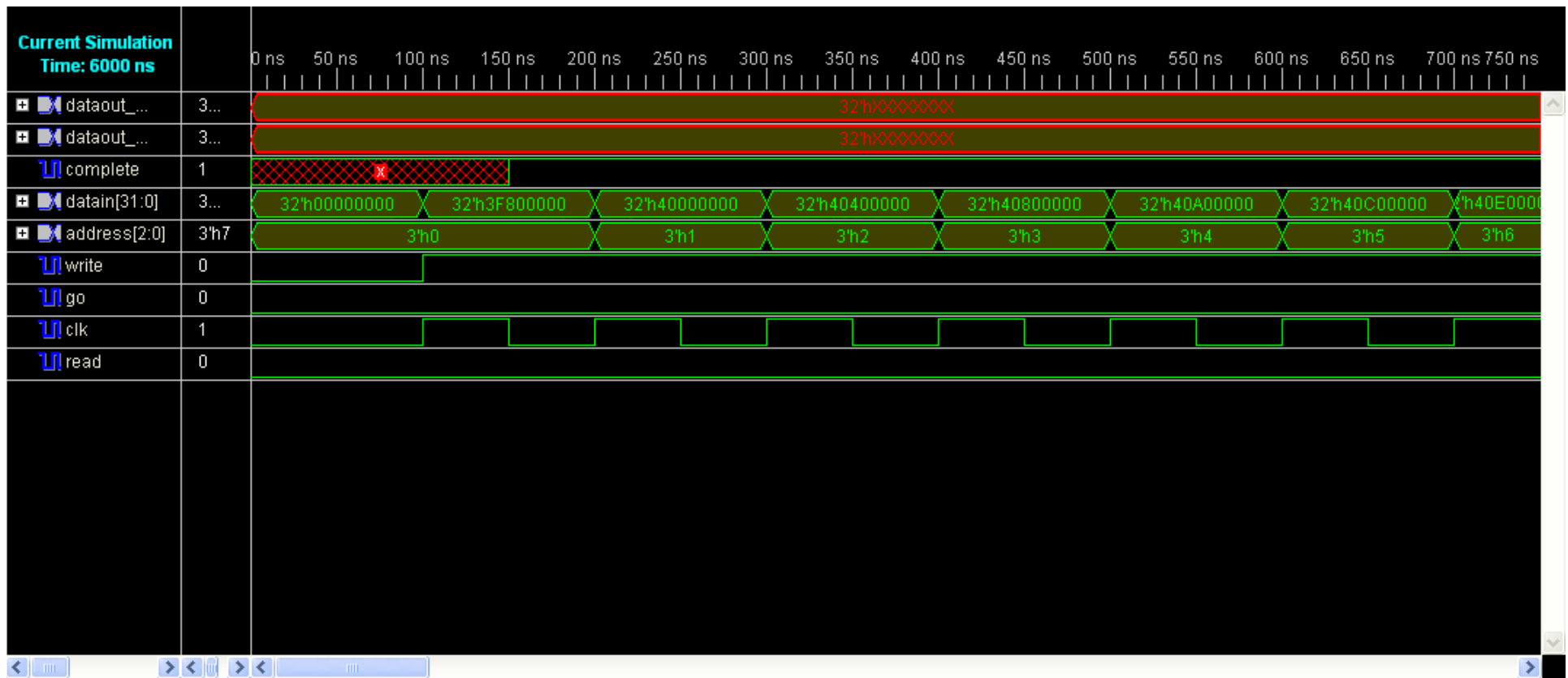


$$(a + bj)(c + dj)$$

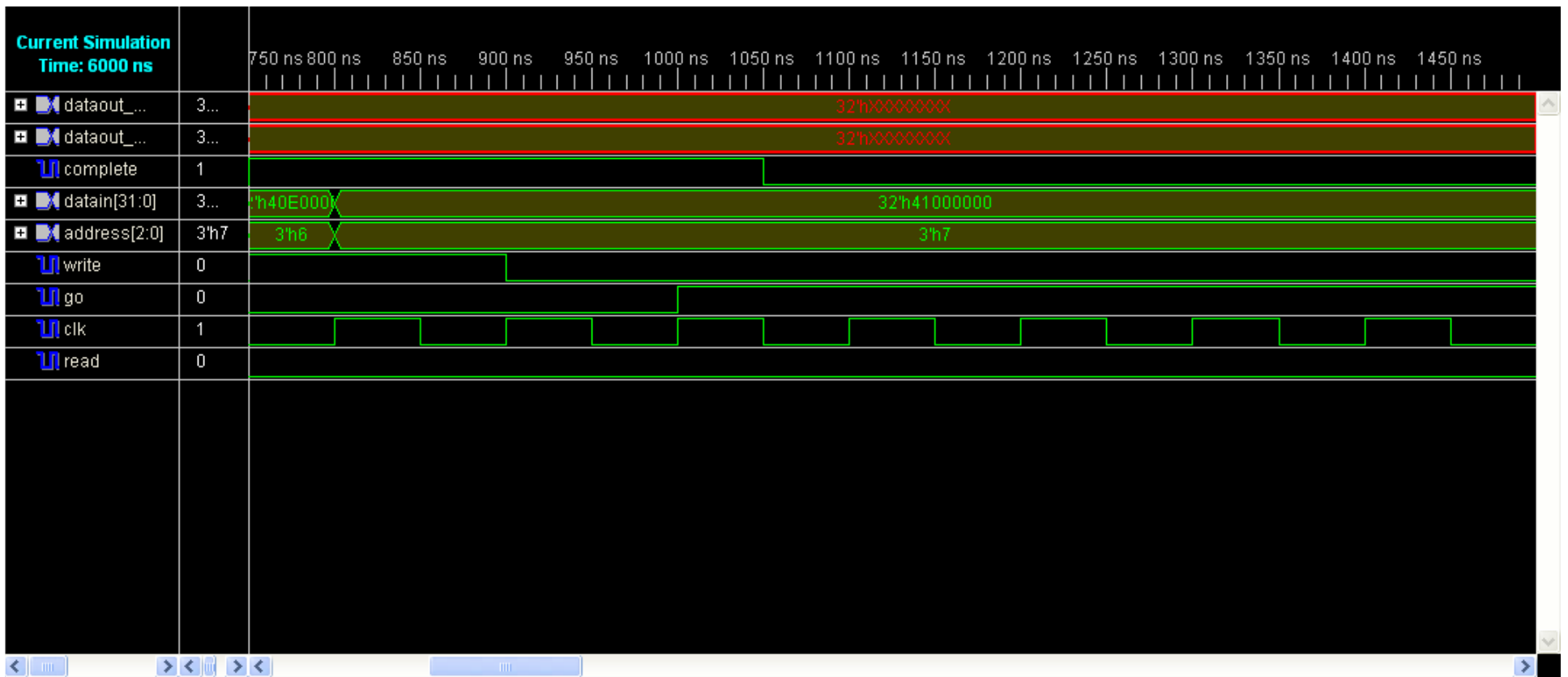
$$ac - bd + adj + bcj$$

$$(ac - bd) + (ad + bc)j$$

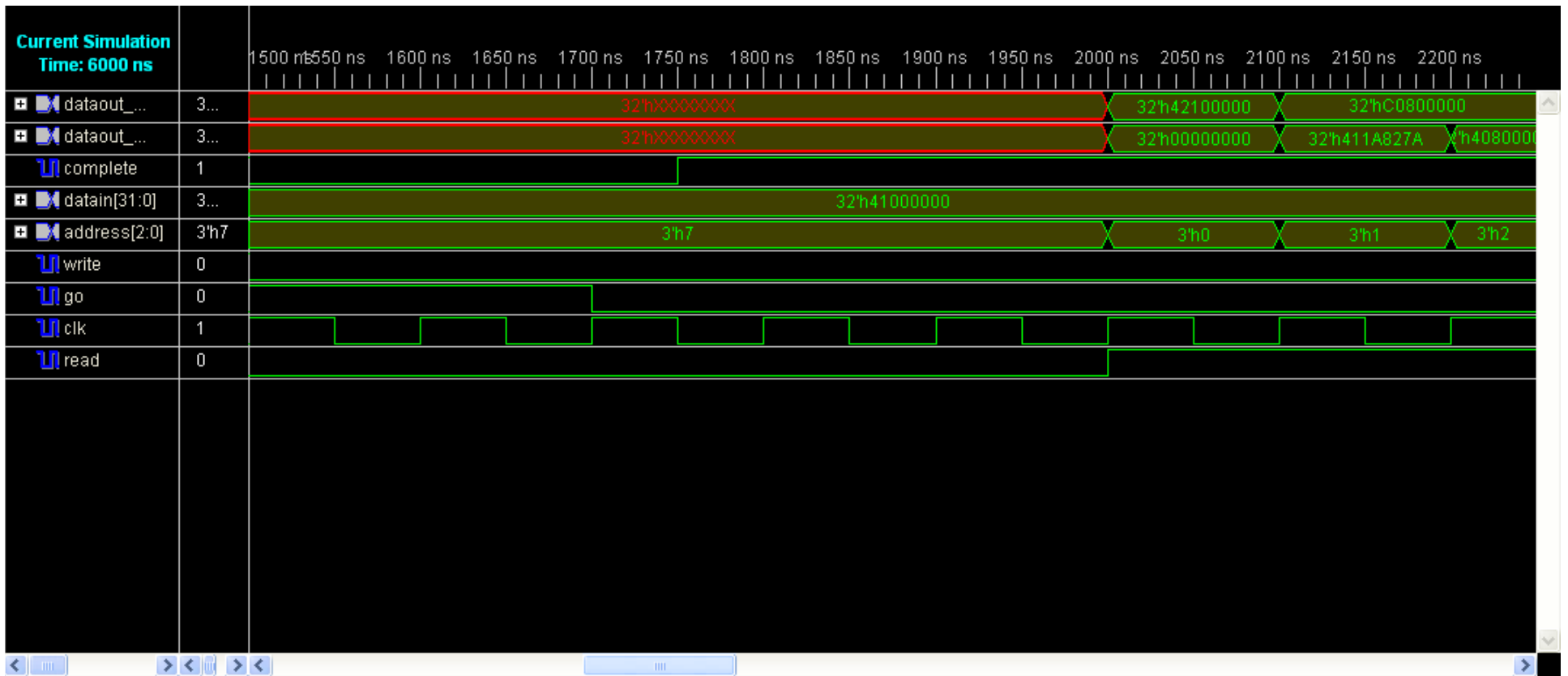
Simulation Waveform



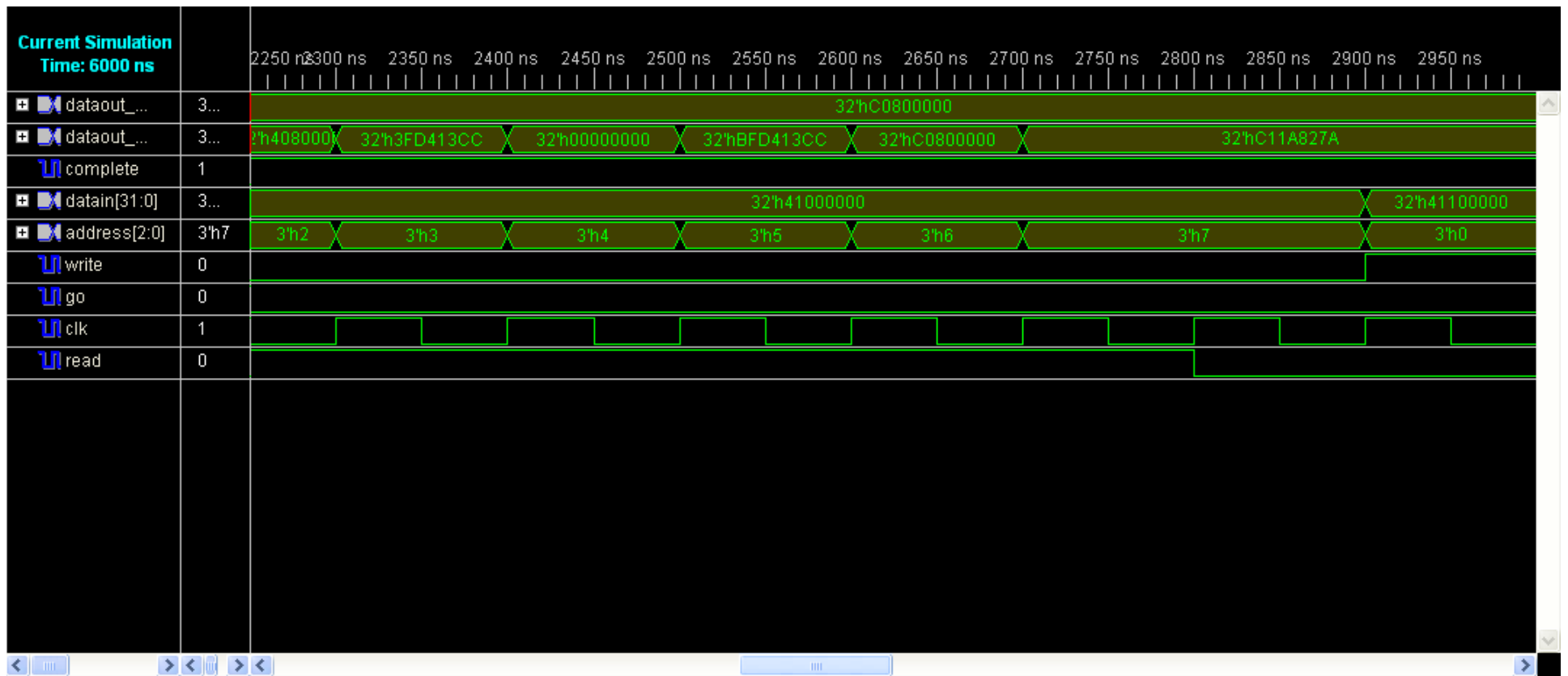
Simulation Waveform – Cont'd



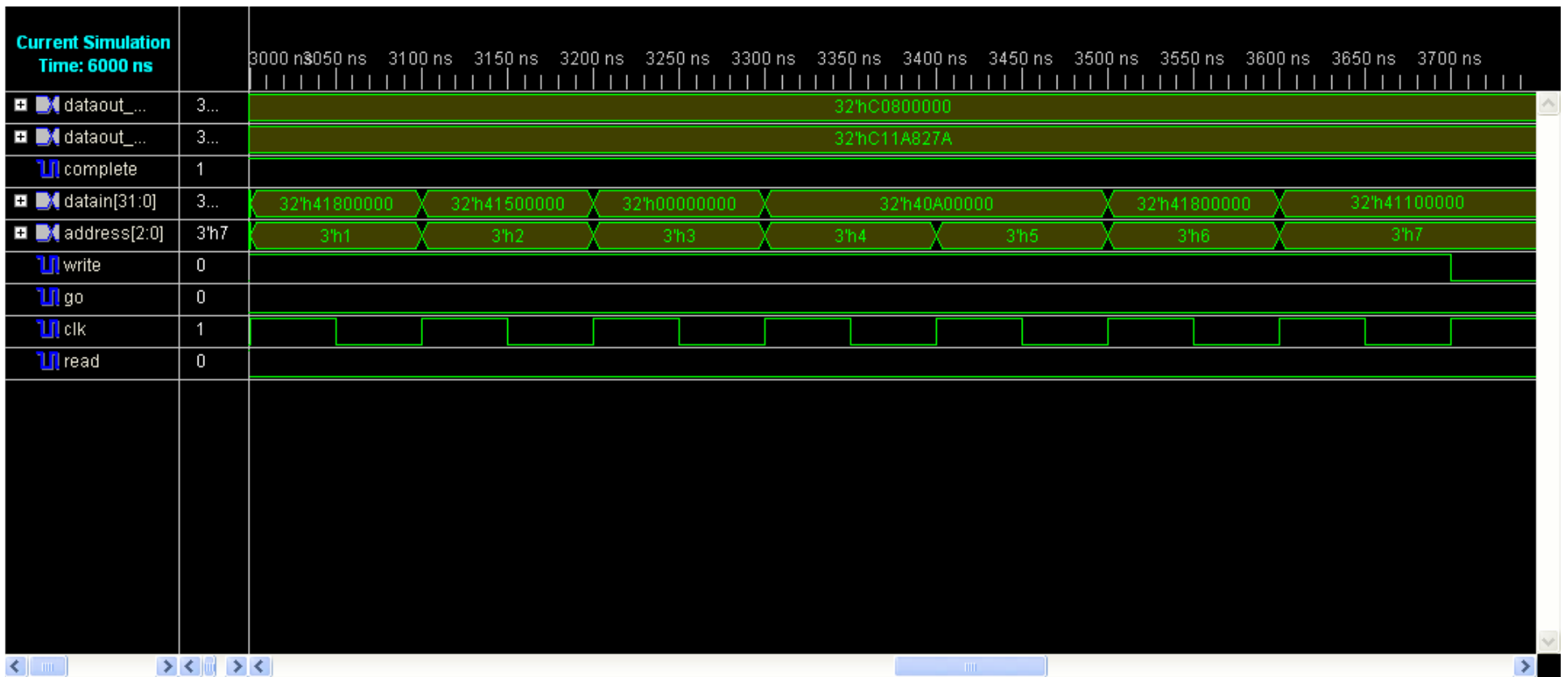
Simulation Waveform – Cont'd



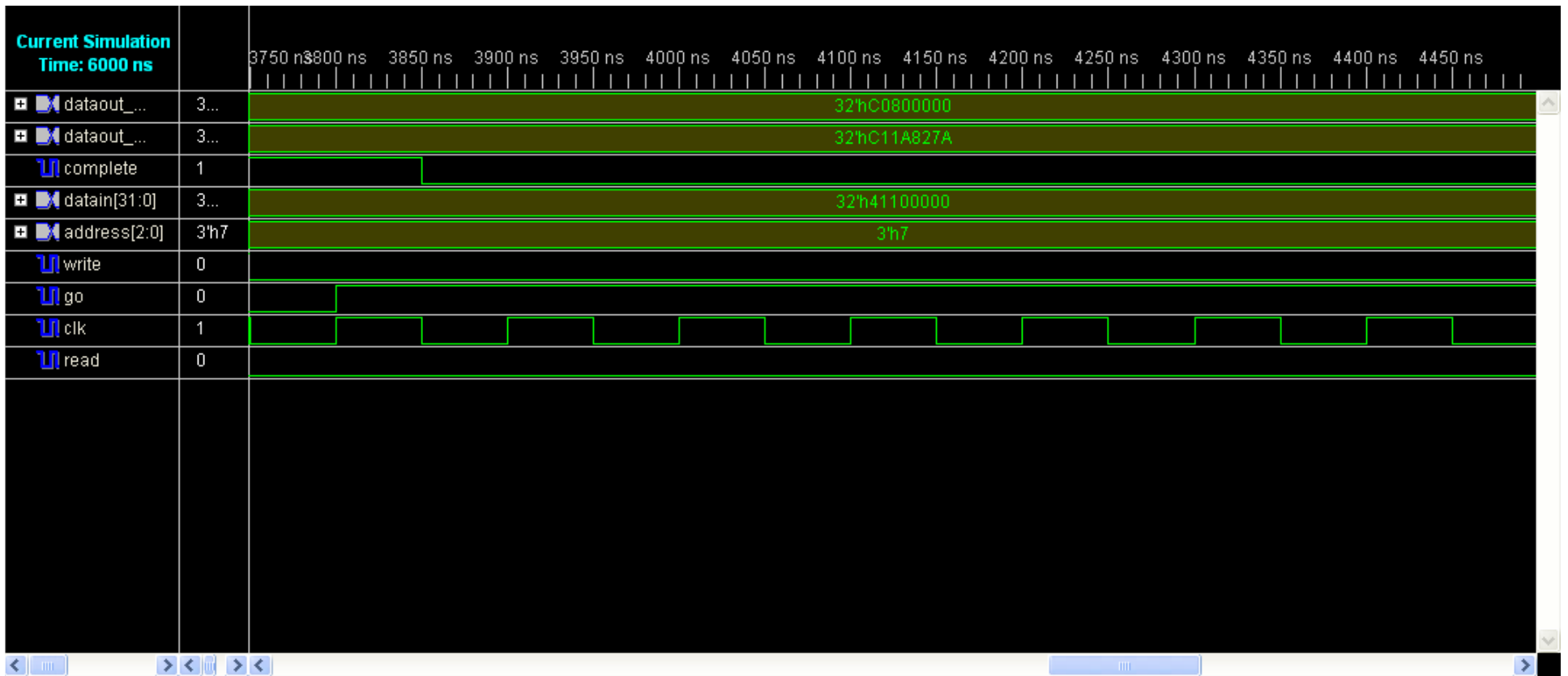
Simulation Waveform – Cont'd



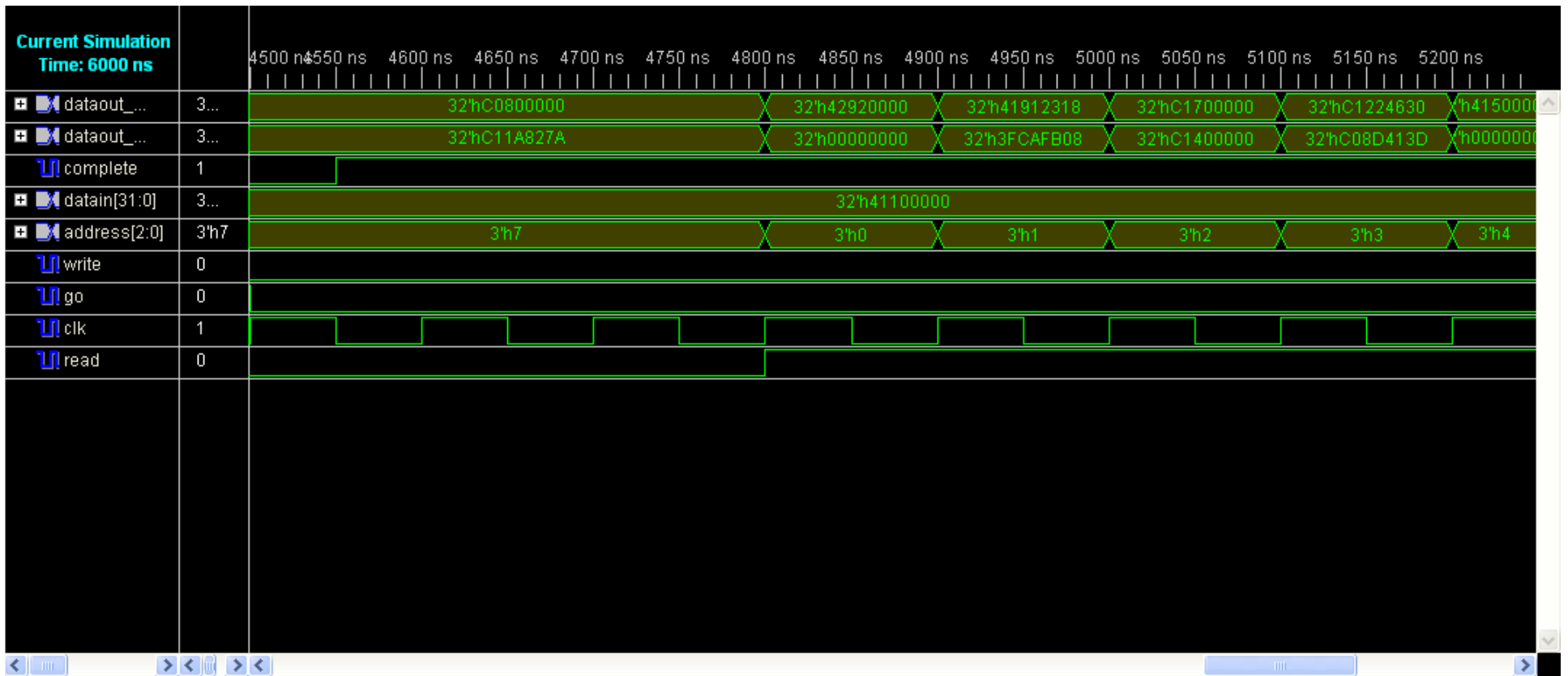
Simulation Waveform – Cont'd



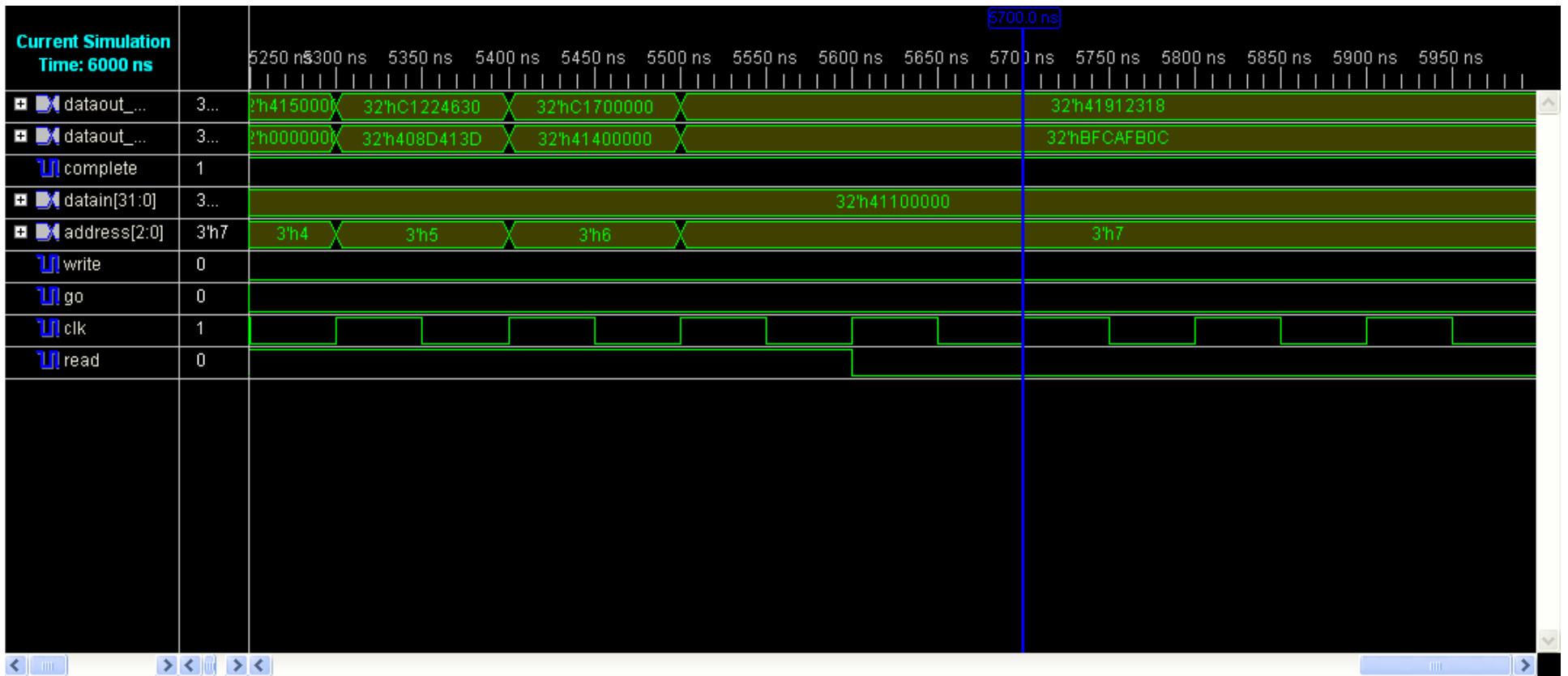
Simulation Waveform – Cont'd



Simulation Waveform – Cont'd



Simulation Waveform – Cont'd



Accuracy Check

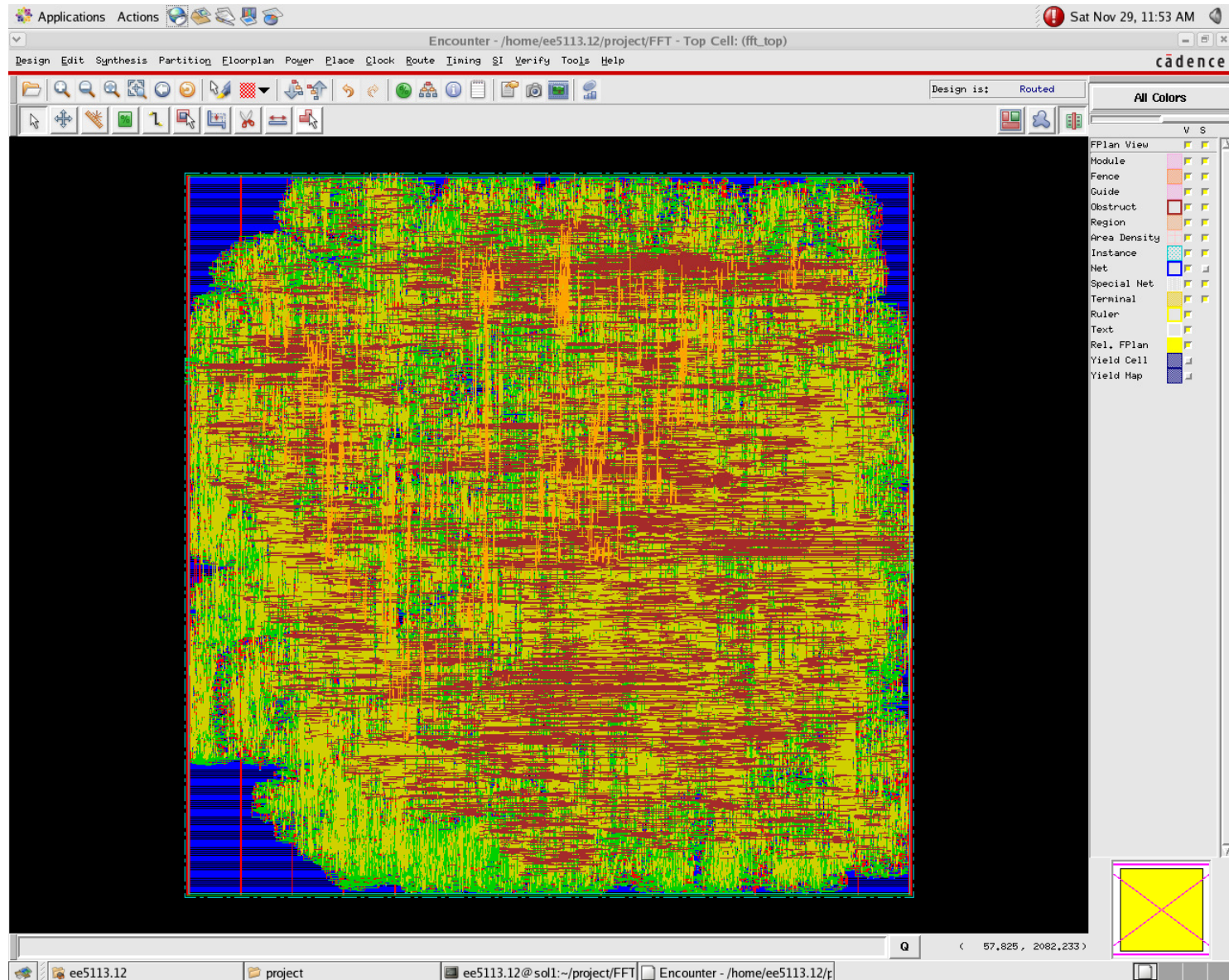
Input Vector		Resultant Vector				
		FFT Result from MatLab	DFT Result using Paired Algorithm from MatLab	DFT Result using Paired Algorithm from simulation		
f ₀	0	36.0000	36.0000	36.0000		F ₀
f ₁	1	-4.0000 + 9.6569i	-4.0000 + 9.6569i	-4.0000 + 9.6569i		F ₁
f ₂	2	-4.0000 + 4.0000i	-4.0000 + 4.0000i	-4.0000 + 4.0000i		F ₂
f ₃	3	-4.0000 + 1.6569i	-4.0000 + 1.6569i	-4.0000 + 1.6569i		F ₃
f ₄	4	-4.0000	-4.0000	-4.0000		F ₄
f ₅	5	-4.0000 - 1.6569i	-4.0000 - 1.6569i	-4.0000 - 1.6569i		F ₅
f ₆	6	-4.0000 - 4.0000i	-4.0000 - 4.0000i	-4.0000 - 4.0000i		F ₆
f ₇	7	-4.0000 - 9.6569i	-4.0000 - 9.6569i	-4.0000 - 9.6569i		F ₇
f ₀	9	73.0000	73.0000	73.0000		F ₀
f ₁	16	18.1421 + 1.5858i	18.1421 + 1.5858i	18.1421 + 1.5858i		F ₁
f ₂	13	-15.0000 - 12.0000i	-15.0000 - 12.0000i	-15.0000 - 12.0000i		F ₂
f ₃	0	-10.1421 - 4.4142i	-10.1421 - 4.4142i	-10.1421 - 4.4142i		F ₃
f ₄	5	13.0000	13.0000	13.0000		F ₄
f ₅	5	-10.1421 + 4.4142i	-10.1421 + 4.4142i	-10.1421 + 4.4142i		F ₅
f ₆	16	-15.0000 + 12.0000i	-15.0000 + 12.0000i	-15.0000 + 12.0000i		F ₆
f ₇	9	18.1421 - 1.5858i	18.1421 - 1.5858i	18.1421 - 1.5858i		F ₇



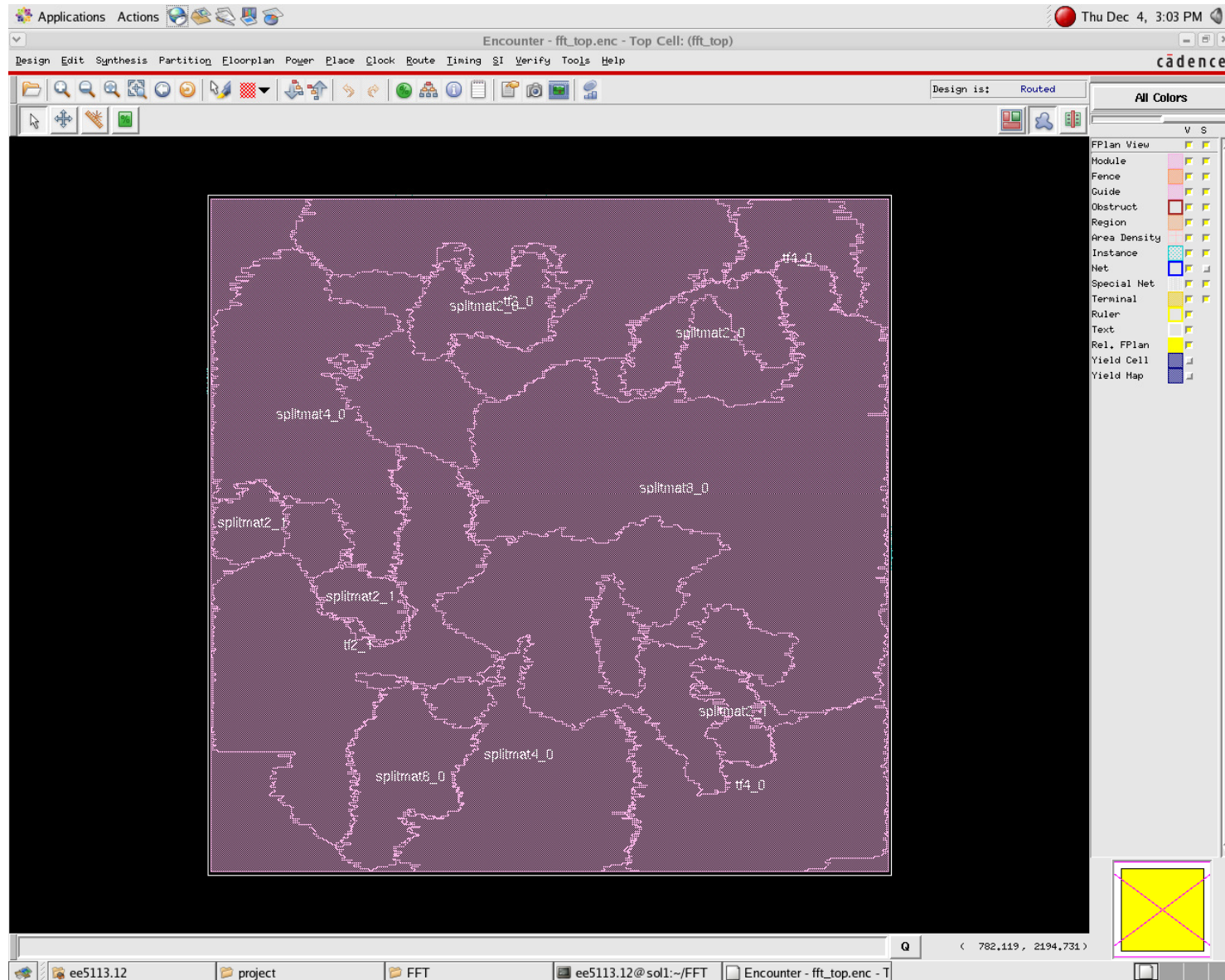
Realization

- Cadence Encounter used to synthesize and create layout
- Used settings and steps outlined in tutorial
 - Core utilization – 0.4
 - Pairs of stripes - 15

Realization



Realization





Realization

■ Number of pins

□ 106

- 32 datain
- 32 dataout real
- 32 dataout imag
- 3 address
- clk
- read, write
- go, complete
- vdd, vss

■ Number of LeafCells

□ 76,580

■ Number of Instances

□ 75,483

■ Number of Gates

□ 163,556

■ Chip Area

□ ~2000 μm x 2000 μm

■ Gate Area

□ 9.9792 μm^2



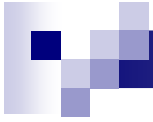
Proposed Optimizations

- Use Complex Conjugate property to reduce hardware
- Reduce number of complex multipliers in twiddle factor modules



Conclusion

- Designing a dedicated DFT circuit, even a relatively small one, is very resource demanding. The designer needs to ensure that all possible optimizations are used to reduce the circuit size.



Thank you!

Questions?